

REMARKS/ARGUMENT

Claims 1-13 are currently pending.

Claim 1 has been amended herein. Applicants make clear that the amendments to claim 1 have not been made for purposes of patentability or to avoid the prior art, but rather were made to correct for minor, non-substantive errors of form. It is respectfully submitted that the amendments do not add new matter and have adequate support throughout the Specification. It is kindly requested that the amendments be entered.

Otherwise, Applicants respectfully traverse all claim rejections and request reconsideration for the following reasons:

I. REJECTIONS OF CLAIMS 1-13 UNDER 35 U.S.C. § 103(a)

Claims 1-3 and 5-13 were rejected under 35 U.S.C. § 103(a) as unpatentable over 5,627,583 to Nakamura et al. (hereinafter "Nakamura") in view of U.S. Patent No. 4,845,555 to Yabe et al. (hereinafter "Yabe"); and claim 4 was rejected under 35 U.S.C. § 103(a) as unpatentable over Nakamura in view of Yabe, and further in view of U.S. Patent No. 6,397,374 to Pasqualini (hereinafter "Pasqualini"). Respectfully, Applicants traverse.

The Examiner asserts that Nakamura discloses every feature of claim 1 except for the delay circuit being "at least partially interposed between said signal source and said first drive signal generator." The Examiner also asserts that Yabe includes such a feature and that it would have been obvious for a person having ordinary skill in the art to modify the Nakamura endoscope with the delay circuit orientation of Yabe "so that the delay circuit is part of the first processor of Nakamura." (Final Office Action, page 3).

Regarding Nakamura, the delay circuit 91 is positioned outside the CPU 75 and FPGA 7. Regarding Yabe, the matching circuit and delay circuit of Figure 10 is located in a connector 7. Thus, a person of ordinary skill in the art could not possibly be motivated by either Nakamura or Yabe to include a delay circuit "as part of said first processor," as recited in claim 1.

Further regarding claim 1, it is respectfully submitted that Yabe does not disclose a delay circuit "at least partially interposed between said signal source and said first drive signal generator." As described immediately above, the matching circuit & delay circuit of Yabe is located in a connector 7, and is disposed between the controller 2 and the endoscope 1. As is readily evident from Yabe, the controller 2 includes all circuitry for sourcing and generating drive signals. In

particular, the control circuit 13 and timing generator 17 constitute a signal generator for driving the endoscope 1, and the CCD drive circuit constitutes a drive signal generator. Thus, unlike claim 1, the matching circuit & delay circuit 34 of Yabe is not interposed between a signal source and a drive generator. Rather, the drive signal generator of Yabe (i.e., the CCD drive circuit 14) is interposed between the matching circuit & delay circuit 34 and the signal source (i.e., control circuit 13 and timing generator 17).

It is noted in Nakamura, et al. that the delay circuit 91 is the one for obtaining the color signals 2R-G and 2B-G by switching the signal subjected to γ correction in the γ correction circuit 90 and the signal having this delayed by 1H by a 1H delay circuit 91 in the 1H switching circuit 93.

On the other hand, it is noted in Yabe, et al. that the matching and delaying circuit 34 is the one provided at the connector section 7 of the endoscope so that various kinds of endoscopes different in lengths of the video signal transmission paths or the like may be connected to the video processor 2.

Hence, the delay circuit for obtaining the color difference signals of 2R-G and 2B-G and the delay circuit provided at the connector section of the endoscope so that various kinds of endoscopes different in lengths of the video signal transmission paths or the like may be connected to the video processor 2 are quite different in their technical purposes. So, we think that a person having ordinary skill in the art does not consider to combine the former and the latter or apply either one of them in place of the other. Thus, we are of an opinion that it is not obvious for a person having an ordinary skill in the art to combine the delay circuit disclosed by Nakamura, et al. and the delay circuit disclosed by Yabe, et al. so as to obtain the constitution in claim 1 of the present application.

It is also noted in Yabe, et al. that the delay circuit is not the one which is built in the video processor as in claim 1 of the present application but the one provided at the connector section of the endoscope to be connected to the video processor.

Thus, since the delay circuit is provided in the video processor in the subject matter of claim 1 of the present application, it is not necessary for every endoscope connected to this video processor to have a delay circuit on its own.

The applicant further notes that in discussing the delay circuit 91 of the primary Nakamura reference, the Examiner refers to that delayed circuit as serving for delaying at least part of signals among signals after video processing. The fact that the delay circuit of this primary reference

processes signals "after video processing" very much determines its structure and purpose and, indeed, the issue whether the teaching of such a delay circuit would be combinable with another reference. The Office Action concedes that the delay circuit of the primary reference is not interposed between the signal source and the first drive signal generator. But the Office Action assumes that one would therefore go to another reference (Yabe, et al.) and draw upon its teaching of a delay circuit which is an entirely different function and which is located the overall apparatus where it would be useless for the purposes of the present invention and combined their teachings. This does not make sense at all.

As regards Pasqualini, any reading of this reference makes clear that it fails to cure the critical deficiencies of Nakamura and Yabe as applied against parent claim 1.

For at least the foregoing reasons, it is respectfully submitted that claim 1 is allowable over Nakamura and Yabe. Furthermore, since claims 2-13 ultimately depend from claim 1, it is respectfully submitted that these claims are allowable over Nakamura and Yabe for at least the same reasons. Accordingly, it is kindly requested that the rejections of claims 1-13 under 35 U.S.C. § 103(a) be withdrawn.

II. CONCLUSION

In view of the foregoing, it is respectfully submitted that all pending claims are currently in allowable condition. Accordingly, reconsideration and prompt allowance of all pending claims is therefore earnestly solicited.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on March 1, 2004

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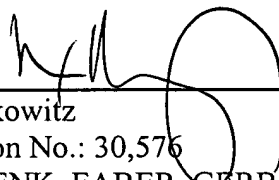
Name of applicant, assignee or
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Signature

March 1, 2004

Date of Signature

Respectfully submitted,



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